

SPI CONTROLLED H-BRIDGE

PRELIMINARY DATA

1 Features

- OPERATING SUPPLY VOLTAGE 5V TO 28V
- TYPICAL $R_{DS(on)} = 150\text{ m}\Omega$ FOR EACH OUTPUT TRANSISTOR (AT 25°C)
- CONTINUOUS DC LOAD CURRENT 5A ($T_{case} < 100^\circ\text{C}$)
- OUTPUT CURRENT LIMITATION AT TYP. 8.6A
- SHORT CIRCUIT SHUT DOWN FOR OUTPUT CURRENTS OVER TYP. 10.6A
- LOGIC- INPUTS TTL/CMOS-COMPATIBLE
- OPERATING-FREQUENCY UP TO 30 kHz
- OVER TEMPERATURE PROTECTION
- SHORT CIRCUIT PROTECTION
- UNDERVOLTAGE DISABLE FUNCTION
- DIAGNOSTIC BY SPI OR STATUS-FLAG (CONFIGURABLE)
- ENABLE AND DISABLE INPUT
- SO20 POWER PACKAGE

2 Description

The L9929 is an SPI controlled H-Bridge, designed for the control of DC and stepper motors in safety critical applications and under extreme environmental conditions.

Figure 1. Package

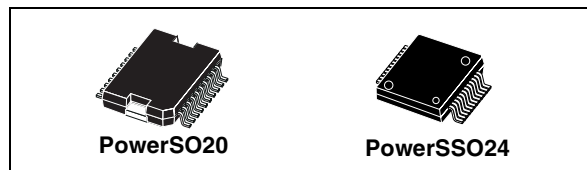


Table 1. Order Codes

Part Number	Package
L9929	PowerSO20
L9929XP	PowerSSO24

The H-Bridge is protected against over temperature and short circuits and has an under voltage lockout for all the supply voltages " V_S " (Main DC power supply). All malfunctions cause the output stages to go tristate.

The H-Bridge contains integrated free-wheel diodes. In case of free-wheeling condition, the low side transistor is switched on in parallel of its diode to reduce the current injected into the substrate. Switching in parallel is only allowed, if the voltage level of the according output-stage is below the ground-level. In this case it must be ensured, that the upper transistor is switched off.

Figure 2. Block Diagram

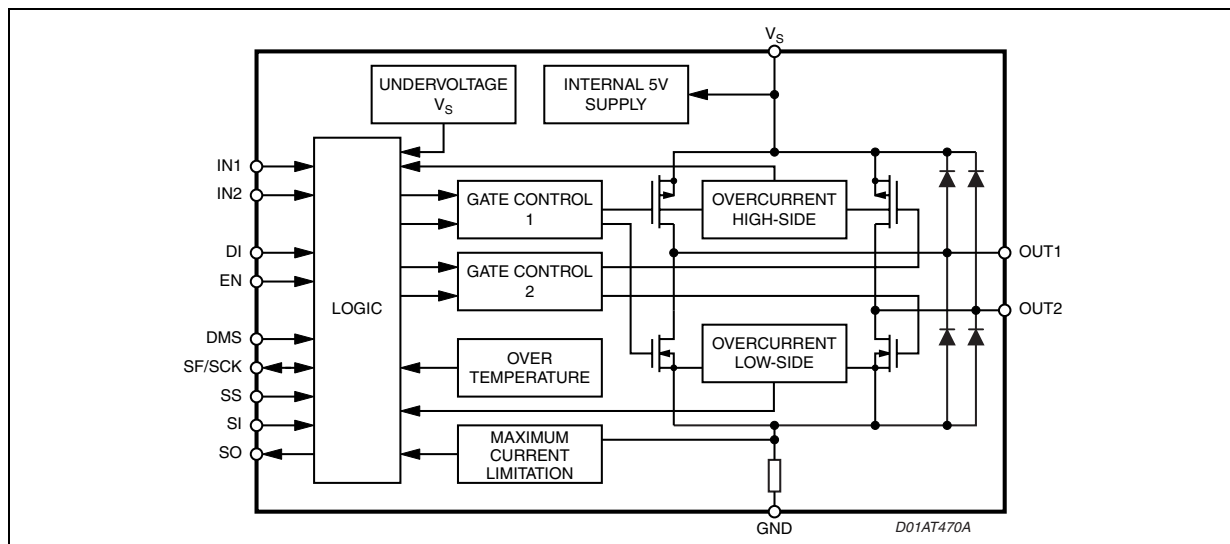


Table 2. Pin Function PowerS020

N°	NAME	Description
1	GND	Ground
2	SCK/SF	SPI-Clock/Status-flag
3	IN1	Input 1
4	V _S	Supply voltage
5	V _S	Supply voltage
6	OU1	Output 1
7	OU1	Output 1
8	SO	serial out
9	SI	serial in
10	GND	Ground
11	GND	Ground
12	DMS	Diagnostic-Mode selection (+ Supply Voltage for SPI-Interface)
13	EN	Enable
14	OU2	Output 2
15	OU2	Output 2
16	V _S	Supply voltage
17	SS	Slave select
18	DI	Disable
19	IN2	Input 2
20	GND	Ground

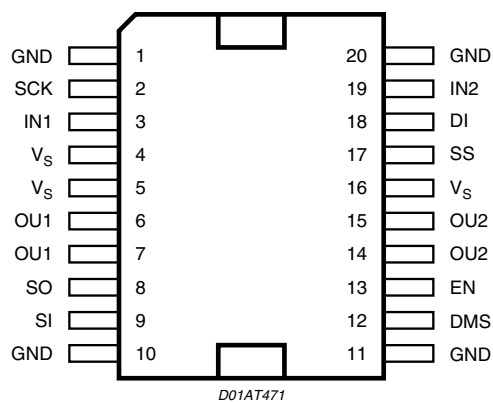
Figure 3. Pin Connection (Top view)

Table 3. Pin Function PowerSS024

N°	NAME	Description
1	GND	Ground
2	SCK/SF	SPI-Clock
3	IN1	Input 1
4	N.C.	Not Connected
5	V _S	Supply voltage
6	V _S	Supply voltage
7	OUT1	Output 1
8	OUT1	Output 1
9	SO	Serial Out
10	SI	Serial In
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	DMS	Diagnostic-Mode selection (+ Supply Voltage for SPI-Interface)
16	EN	Enable
17	OUT2	Output 2
18	OUT2	Output 2
19	V _S	Supply voltage
20	SS	Slave select
21	DI	Disable
22	IN2	Input 2
23	N.C.	Not Connected
24	GND	Ground

Figure 4. Pin Connection (Top view)

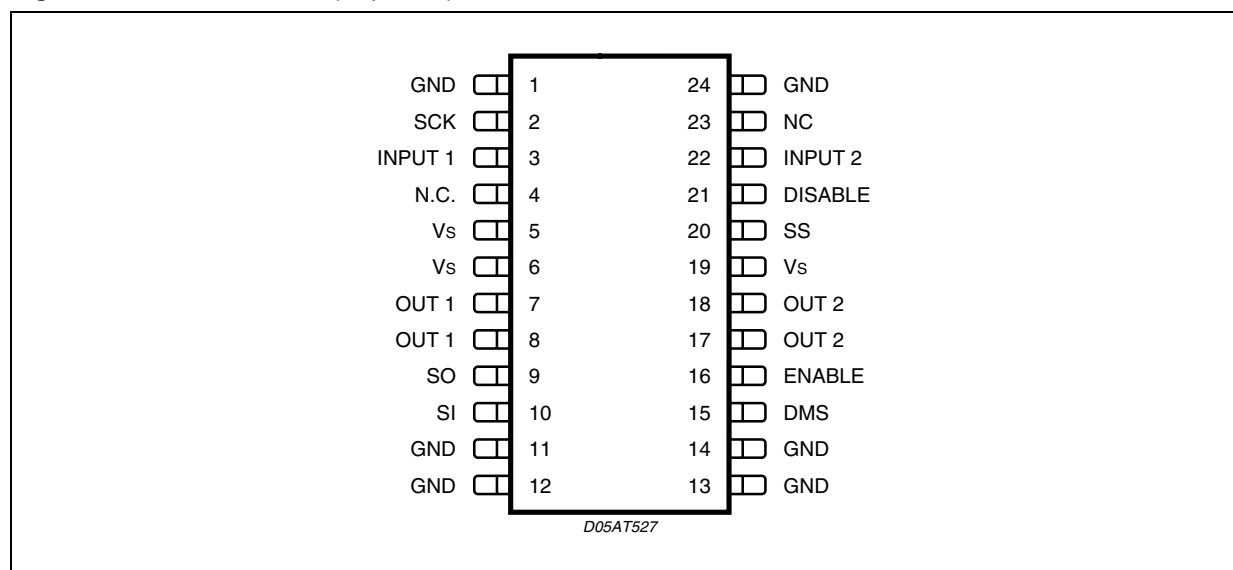


Table 4. Absolute Maximum Ratings

The integrated circuit must not be destroyed by use at the limit values.

Each limit value can be used, as long as no other limit is violated.

Voltage reference point: All values are, if not otherwise stated, relative to ground.

Direction of current flow: Current flow into a pin is positive.

Rise-, fall- and delaytimes: If not otherwise stated, all rise times are between 10% and 90%, fall times between 90% and 10% and delay times at 50% of the relevant steps.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _S	Supply voltage	static destruction proof	-1		40	V
		dynamic destruction proof t < 0.5s (single pulse, T _j < 85°C)	-2		40	V
V _{LI}	Logic inputs IN1, IN2, DI, EN, SS, SI, SCK, DMS		-0.5		7	V
V _{LO}	Logic outputs SF, SO		-0.5		7	V

Table 5. Thermal Data

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T _j	Junction temperature		-40		+150	°C
		dynamic t < 1 s			+175	°C
T _{stg}	Storage temperature		-55		+125	°C
T _{amb}	Ambient temperature		-40		+125	°C
R _{th j-case}	Thermal resistance junction to case (*)				3	°C/W
T _{j_sd}	Thermal Shutdown Junction Temperature Threshold		160	175	190	°C
T _{j_reg}	Start of Temperature dependent Current Regulation		150	165	180	°C

(*) Guaranteed by design and package characterization.

Table 6. Electrical Characteristics

(T_j = -40 to +150°C; V_S = 5 to 28V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY						
V _S	Supply Voltage	Static Condition	4.5		28	V
		Dynamic Condition (t < 500ms)			40	V
	Undervoltage Shutdown	(at least down to 2.5V) (*)				
	Switch OFF voltage				4.4	V
	Switch ON voltage				4.7	V
	Hysteresis			200		mV
V _{DMS}	SPI Undervoltage Shutdown	Device used in SPI mode	2.5	2.8	3.1	V
I _S	Supply current	f = 0 kHz, I _O = 0 A			13	mA
		f = 20kHz, I _O = 0 A			30	mA

(*) For supply voltages down to 2.5V the output stages are in tristate condition and the status flag is set to low. Below 2.5V the device operates in undefined condition

Table 6. Electrical Characteristics (continued)($T_j = -40$ to $+150^\circ\text{C}$; $V_S = 5$ to 28V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Logic inputs						
V _{IH}	Logic Input Voltage High IN1, IN2, DI, EN		2.14			V
V _{IL}	Logic Input Voltage Low IN1, IN2, DI, EN				0.86	V
V _H	Logic Input Voltage Hysteresis IN1, IN2, DI, EN		0.1		0.6	V
I _I	Logic Input Current IN1, IN2, DI	V _I ≤ 1V	-200	-125		μA
I _{EN}	Logic Input Current EN	V _{IEN} ≥ 1V			100	μA
t _{dt}	Detection Time EN, DI			3	4	μs
Power Outputs (OUT1, OUT2)						
R _S	Switch on Resistance LS	R _{OUT-VS} , V _S > 5 V		150	250	mΩ
	Switch on Resistance HS	R _{OUT-GND} , V _S > 5 V		150	250	mΩ
I _{OULmax}	Switch-off Current (*)	-40 °C < T _j < 165 °C T _j < 175 °C	7.8	8.6 2.5	10.5(tbd)	A A
t _a	Switch-off time		12	17	22	μs
t _b	Blanking time		8	11.5	15	μs
t _a /t _b	Tracking		1.3	1.5	1.7	
I _{LOUK}	Short circuit detection current (*)		8.9	10.6	-	A
ΔI _{LOUK}	Short Circuit Current Trecking (*)		1.3	2.0	-	A
t	Reactivation time after internal shut down	Overcurrent- or overtemperature shut down to reactivation of the output stage			200	μs
I _L	Leakage Current	Output stage switched off			1	mA
V _{FD}	Free-wheel diode forward voltage	I _O = 3A, V _S = 0V			2	V
I _{SF}	Output„high“ (SF not set)	V _{SF} = 5V			20	μA
I _{SF}	Output„low“ (SF set)	V _{SF} = 0.5V	350			μA
		V _{SF} = 0.8V	400			μA
		V _{SF} = 1V	400			μA
Timing						
f	Maximum PWM Frequency	min. operating time 10μs Device can not be controlled with higher frequency (specify in max ratings?)		2	30	kHz
f _S	Switching Frequency during current limitation	f = 1/(t _a +t _b)		20	50	kHz
t _{don}	Output ON-delay	IN1 --> OUT1 or IN2 --> OUT2		3	7.5	μs
t _{doff}	Output OFF-delay			3	5	μs
t _r	Output rise time	OUT1H--> OUT1L, OUT2H--> OUT2L, I _{OUT} = 3 A OUT1L--> OUT1H, OUT2L--> OUT2H		1	5	μs
t _f	Outout fall time			1	3	μs
t _{ddis}	Disable Delay Time	DI --> OUTn, En --> OUTn		3	7	μs
t _{dp}	Power on Delay Time	V _S = on --> output stage active			1	ms
t _{err}	Delay time for fault detection		1		6	μs

(*) In case of SC OUTx to gnd resp. to V_S the SC switch off current is always higher than the start value of current regulation ($\Delta I_{LOUK} = I_{LOUK} - I_{LOUmax}$)

The diagram shows two digital signals, IN_n and OUT_n , over time. IN_n is a square wave with a 50% duty cycle. OUT_n is a square wave with a 90% duty cycle. The output OUT_n transitions from high to low when IN_n transitions from high to low, and from low to high when IN_n transitions from low to high. The time delay between the input transition and the output transition is labeled t_{don} (for the low-to-high transition) and t_{doff} (for the high-to-low transition).

The diagram shows a trapezoidal waveform for the signal OUT_n . The signal transitions from a low level to a high level with a 90% rise time and returns to the low level with a 90% fall time. The pulse width is 10% of the period. The time intervals for the rise and fall are labeled t_f and t_r respectively. The identifier D01AT474 is present in the bottom right corner.

The diagram shows three waveforms over time:

- LOAD CURRENT:** Starts at 0, rises to a peak labeled "typ. 10.6 A", then settles into a steady-state oscillation around "typ. 8.6 A". A dashed line indicates the "OVERCURRENT" threshold. A region of the oscillation is labeled "CURRENT LIMITATION PHASE". An arrow points to the start of this phase with the text "Reaching Switch-off current, limitation phase is started by triggering t_b ".
- CONTROL SIGNAL:** A step function that transitions from low to high at the start of the current limitation phase and returns to low at the end of the overcurrent event.
- STATUS FLAG:** A pulse that is active (high) during the current limitation phase and the subsequent overcurrent event.

DETAIL A

This detail shows a close-up of the current limitation phase. It illustrates the relationship between the current waveform and the timing parameters t_a and t_b .

- t_a is the "SWITCH_OFF TIME IN CURRENT LIMITATION", shown as the time from the start of the current limitation phase to the point where the current begins to decay.
- t_b is the "CURRENT LIMITATION BLANKING TIME", shown as the time from the start of the current limitation phase to the point where the current returns to the steady-state level.

The diagram also shows the "OVERCURRENT DETECTION" threshold, which is a dashed line above the steady-state current level.

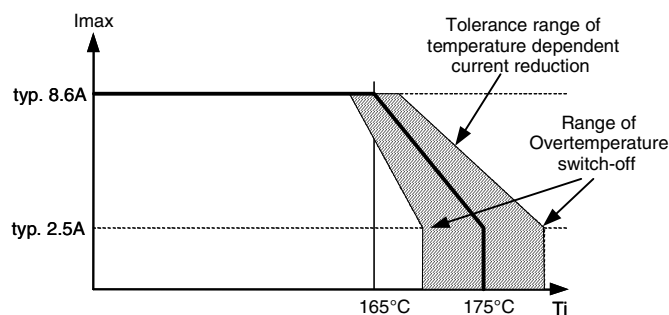
Figure 9.

Temperature-depending current-limitation

Maximum rating for junction temperature

Overtemperature switch-off

Switch-off current in case of current limitation

For typical $165^{\circ}\text{C} < T_j < 175^{\circ}\text{C}$ the maximum current decreasesfor $< 1\text{ s } 175^{\circ}\text{C}$ $> \text{typ. } 175^{\circ}\text{C}$ typ. 8.6A $T_j < \text{typ. } 165^{\circ}\text{C}$ **Table 5. Electrical Characteristics (continued)****Spi Interface**

The timing of L9929 is defined as follows:

- The change at output (SO) is forced by the rising edge of the SCK signal.
- The input signal (SI) is taken over on the falling edge of the SCK signal.
- $\overline{\text{SS}} = \text{active}$ without any clocks at SCK is not allowed
- The data received during a writing access is taken over into the internal registers on the rising edge of the $\overline{\text{SS}}$ signal, if exactly 16 SPI clocks have been counted during $\overline{\text{SS}} = \text{active}$.

Figure 10.

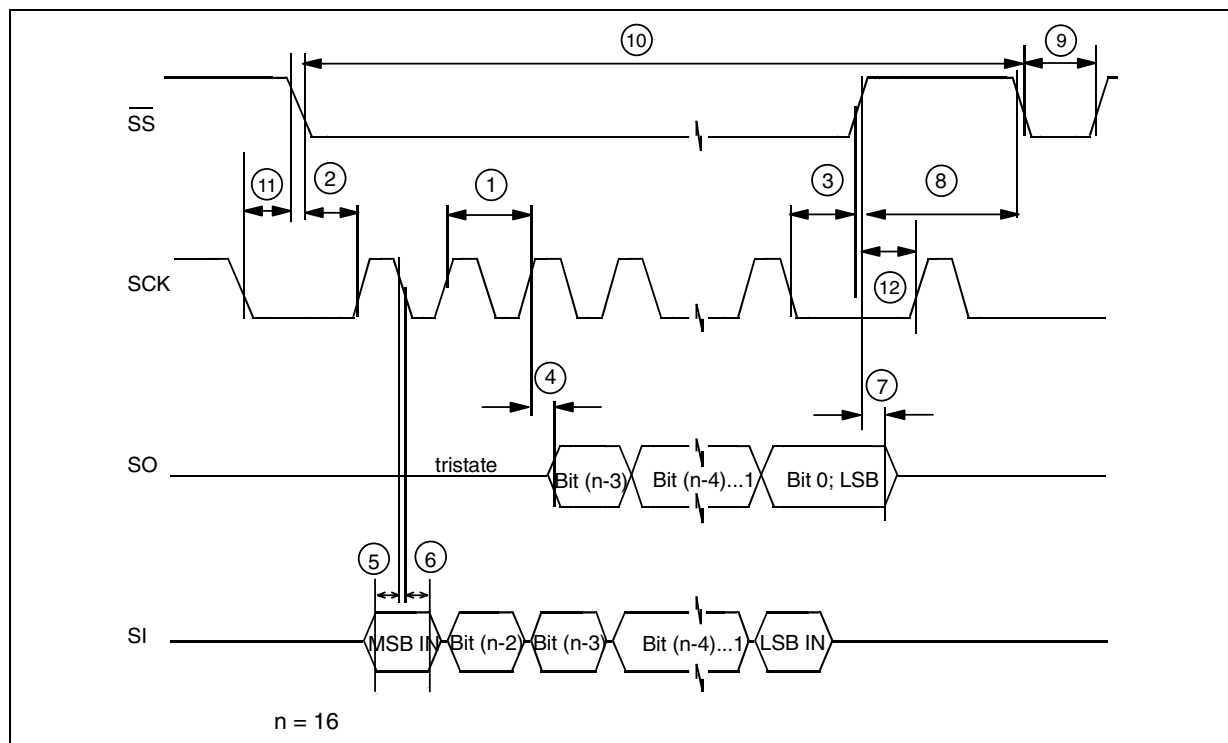


Table 5. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input SCK (SPI clock input)						
V _{SCKL}	Low Level				1	V
V _{SCKH}	High Level		2			V
ΔV _{SCK}	Hysteresis		0.1		0.4	V
C _{SCK}	Input Capacity				10	pF
-I _{SCK}	Input Current	Pull up current source connected to V _S		20	50	μA
Input SS (Slave select signal)						
V _{SSL}	Low Level	L9929 is selected			1	V
V _{SSH}	High Level		2			V
ΔV _{SS}	Hysteresis		0.1		0.4	V
C _{SS}	Input Capacity				10	pF
-I _{SS}	Input Current	Pull up current source connected to V _S		20	50	μA
Input SI (SPI data input)						
V _{SIL}	Low Level				1	V
V _{SIH}	High Level		2			V
ΔV _{SI}	Hysteresis		0.1		0.4	V
C _{SI}	Input Capacity	Guaranteed by design			10	pF
-I _{SI}	Input Current	Pull up current source connected to V _S		20	50	μA
Output SO (Tristate output of the L9929 (SPI output); On active reset (DI) output SO is in tristate.)						
V _{SOL}	Low Level	I _{SO} = 2mA			1	V
V _{SOH}	High Level	I _{SO} = -2mA	2			V
C _{SO}	Capacity	Capacity of the pin in tristate			10	pF
-I _{SO}	Leakage Current	In tristate	-10		10	μA
Input DMS (Supply-Input for the SPI-Interface and Selection Pin for SPI- or SF-Mode)						
V _i	Input Voltage	SPI-Mode Status-Flag-Mode	4.5		0.8	V V
I _c	Input Current	SPI-Mode			10	mA
Timing						
t _{cyc}	Cycle-Time (1)		200			ns
t _{lead}	Enable Lead Time (2)		100			ns
t _{lag}	Enable Lag Time (3)		150			ns
t _v	Data Valid CL = 40pF (4) Data Valid CL = 200pF (referred to L9929)				40 150	ns ns
t _{su}	Data Setup Time (5) (referred to master)		50			ns
t _h	Data Hold Time (6)		20			ns
t _{dis}	Disable Time (7) (referred to L9929)				100	ns

Table 5. Electrical Characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{dt}	Transfer Delay (8) (referred to master)		150			ns
t_{SCKH}	Serial clock high time (9) (referred to master)		50			ns
t_{SCKL}	Access time (10) (referred to master)		8.35			μ s
	Clock inactive before chipselect becomes valid (11)		200			ns
	Clock inactive after chipselect becomes valid (12)		200			ns
t_{rs}	Rise-, fall time	Load on SO 50pF	20			ns
TIMING						
	Diagnostic Threshold (Open Load Detection DMS > 3.1V, EN < 18V and/or DI > 2V)					
V _{OUT1} V _{OUT2}		Load is available	0.8 0.8			V V
V _{OUT1} V _{OUT2}		Load is missing	1		V _S 0.8	V V
I _{OUT2} I _{OUT1}	Diagnostic Current	DMS > 3.1V, EN < 0.8V EN < 18V and/or DI > 2V	700 1000	1000 1500	1350 2000	μ A μ A
	Tracking Diagnostic Current	I _{OUT1} / I _{OUT2}	1.4	1.5	1.6	
t_D	Delay Time	* After disabling the device, the load has to be demagnetized during t _D ,to avoid erroneous OL detection	30		100	ms

3 Truth Table

Table 7. Truth Table

Pos.	DI	EN	IN1	IN2	OUT1	OUT2	SF ³⁾	SPI ⁴⁾ DIA_REG
1. Forward	L	H	H	L	H	L	H	See Diagnostics /Encoding of Failures
2. Reverse	L	H	L	H	L	H	H	
3. Free-wheeling low	L	H	L	L	L	L	H	
4. Free-wheeling high	L	H	H	H	H	H	H	
5. Disable	H	X	X	X	Z	Z	L	
6. Enable	X	L	X	X	Z	Z	Z	
7. IN1 disconnected	L	H	Z	X	H	X	H	
8. IN2 disconnected	L	H	X	Z	X	H	L	
9. DI disconnected	Z	X	X	X	Z	Z	L	
10. EN disconnected	X	Z	X	X	Z	Z	L	
11. Current limit. active	L	H	X	X	Z	Z	H	
12. Undervoltage active ^{1.)}	X	X	X	X	Z	Z	L	
13. Overtemperature ^{2.)}	X	X	X	X	Z	Z	L	
14. Overcurrent ^{2.)}	X	X	X	X	Z	Z	L	

- 1.) In case of undervoltage tristate and status-flag are reset automatically.
- 2.) Whenever overcurrent or overtemperature is detected, the fault is stored (i.e. status-flag remains low).
The tristate conditions and the status-flag ³⁾ are reset via DI or EN.

L = Low

H = High

X = High or Low

Z = High impedance

(all output stage transistors are switched off in static state. For more inform. see next page)

Overcurrent: $I_{OUT1,2} > 10.6 \text{ A}$

Overttemperature: $T_j > 175^\circ\text{C}$

Undervoltage: $V_{VS-GND} < 4.5\text{V}$ (at least down to 2.5V)

- 3.) If Mode „Status-Flag“ is selected (see chapter "Diagnostic / Status-Flag")
- 4.) If Mode „SPI-Diagnosis“ is selected (see chapter "Diagnostic / SPI-Interface")

Description of the state „Z“

The state „Z“ has, depending on the previous operating condition different meaning.

1. dynamical

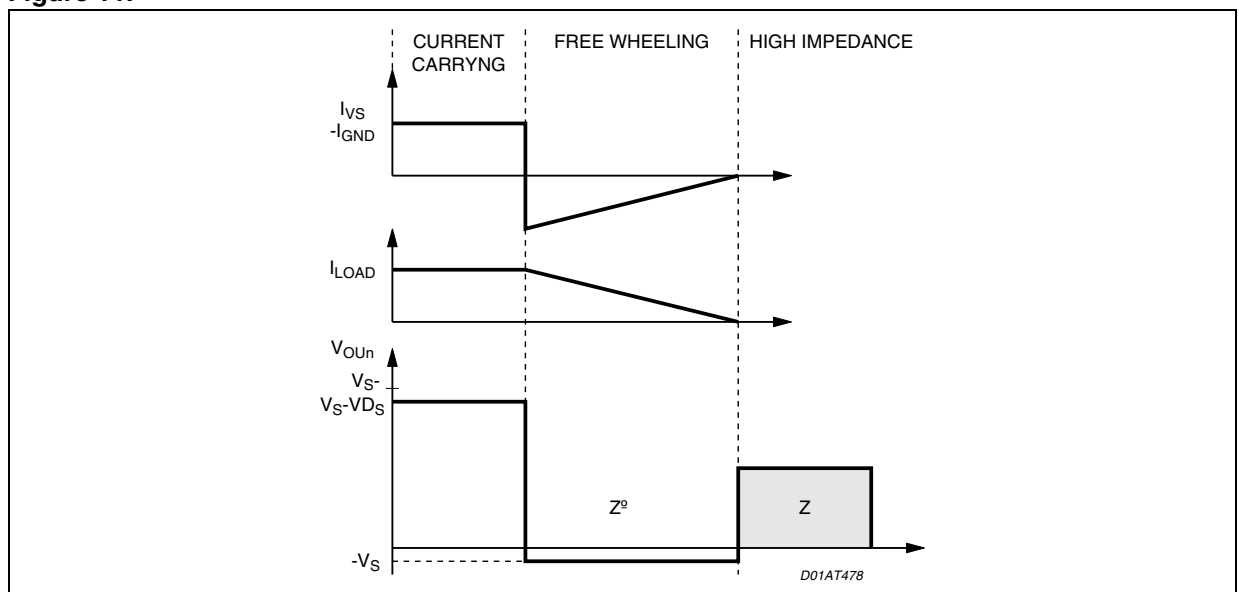
I. e. the inductive load is current carrying and is switched off according to Pos. 5, 6, 9, 10, 11, 12, 13, or 14 of the truth table

- a.) All output stage transistors are switched off.
- b.) The current flow is continued via the free wheeling diodes.
- c.) Free wheeling is detected by a negative voltage-level at OUn.
- d.) Switch on of the parallel-transistor of the current carrying diode.
- f.) Free wheeling is finished, if the voltage-level on OUn is positive again.

2. statical

- g.) all output-stages switched off.

Figure 11.



4 Diagnostic

The Diagnosis-Mode can be selected between SPI-Diagnosis and Status-Flag Diagnosis.

The choice of the Diagnosis-Mode is selected by the voltage-level on pin 12 (DMS Diagnosis Mode Selection).

DMS = GND Status-Flag

DMS = Vcc SPI-Diagnostic

For the connection of pins SI, SO, SS and SCK/SF see Fig. 13 respectively Fig. 14.

4.1 Status-Flag

The Status-Flag shows the condition „tristate“.

At the following fault-cases the output-stages switches in tristate and set the status-flag from high to low.

- Short circuit of OUT1 or OUT2 against V_S or GND
- Short circuit between OUT1 and OUT2
- Overcurrent
- Overtemperature
- Undervoltage on V_S

In cause of short circuit or overcurrent, the fault will be stored.

The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.

If the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of overtemperature the fault will be stored.

The output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is exceeded.

If the voltage level changes from high to low on DI or from low to high on EN, the output stage switches on again and the status-flag is reset to high-level.

In cause of undervoltage on V_{Batt} the output stage switches in tristate and the status-flag is set from high level to low-level if the specified value is fallen. If the voltage has risen about the specified value again, the output stage switches on again and the status-flag is reset to high-level.

The maximum current which can flow under normal operating conditions is limited to typical $I_{max.} = 8.6A$.

When the maximum current value is reached, the output stages are switched tristate for a fixed time.

According to the time-constant the current decreases exponentially until the next switch-on occurs.

At the end if the fixed time the output stage switches on again and the status-flag is reset to high-level.

5 SPI-INTERFACE

5.1 General Discription

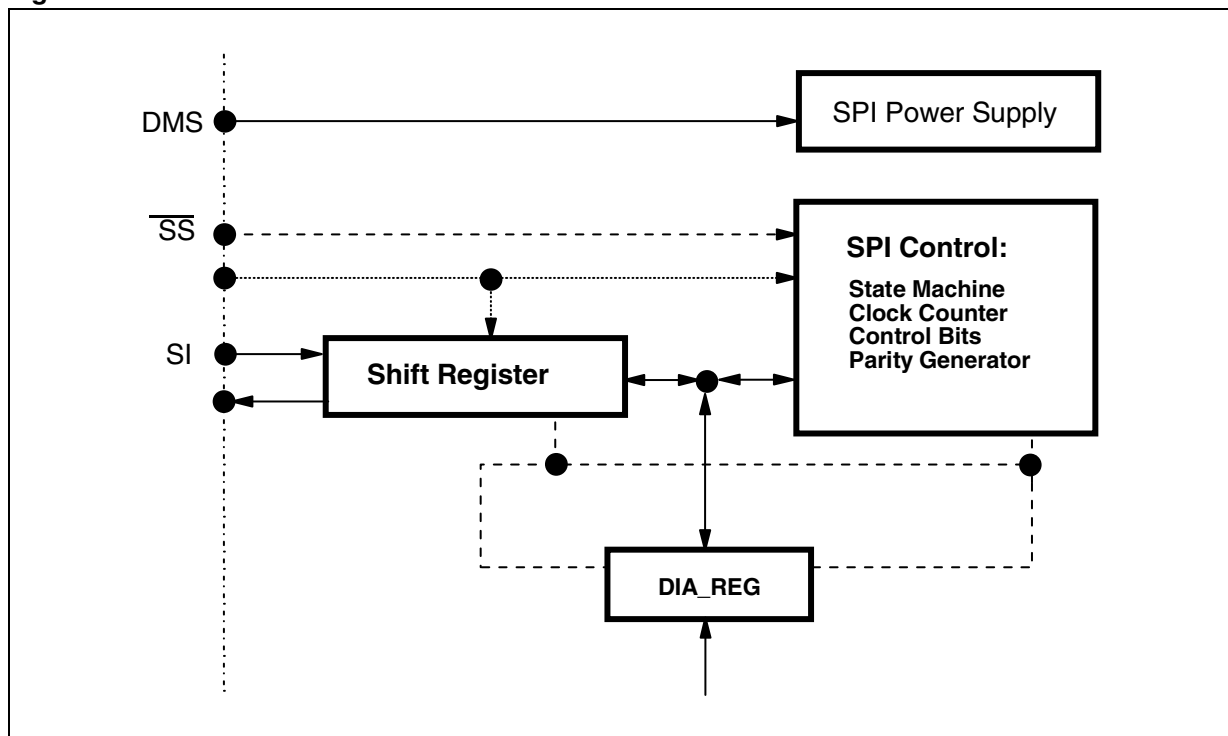
The serial SPI interface establishes a communication link between L9929 and the systems microcontroller. L9929 always operates in slave mode whereas the controller provides the master function.

The maximum baud rate is 2 Mbaud (200pF).

Applying an active slave select signal at SS L9929 is selected by the SPI master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.

In case of inactive slave select signal (High) the data output SO goes into tristate.

Figure 12.



5.2 Power Supply of the SPI-Interface

SPI-Logic and I/O-Pins are alternatively supplied from DMS or Vcc internal, depending on which voltage is higher. That is why diagnosis of the EN-/DI-Pins is always possible, even in case of missing H-Bridge-power supply e.g. during „Vorlauf/Nauchlauf“.

5.3 Characteristics of the SPI Interface

- 1) When DMS is > 3.1V, the SPI is active, independent of the state of EN or DI and the voltage on V_S. During active reset conditions (DMS < 2.5V) the SPI is driven into its default state. When reset becomes inactive, the state machine enters into a waitstate for the next instruction.
- 2) If the slave select signal at SS is inactive (high), the state machine is forced to enter the waitstate, i.e. the state machine waits for the following instruction.
- 3) During active (low) state of the select signal SS the falling edge of the serial clock signal SCK will be used to latch the input data at SI. Output data at SO are driven with the rising edge of SCK. Further processing of the data according to the instruction (i.e. modification of internal registers) will be triggered by the rising edge of the SS signal. (-> See Note)
- 4) Chipaddress: In order to establish the option of extended addressing the uppermost two bits of the instruction-byte (i.e the first two SI-bits of a Frame) are reserved to send a chipaddress. To avoid a busconflict the output SO must stay high impedant during the addressing phase of a frame (i.e. until the addressbits are recognised as valid chipaddress). This tristate behavior should be realised in any case, regardless whether the extended addressoption is used or not. If the chipaddress does not match, the according access will be ignored and SO remains high impedant for the complete frame regardless which frametype is applied.
- 5) Check byte: Simultaneously to the receipt of an SPI instruction L9929 transmits a check byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial bitpattern and a flag indicating an invalid instruction of the previous access.

- 6) On the read access the databits at the SPI input SI are rejected.
- 7) Invalid instruction/access: An instruction is invalid, if one of the following conditions is fulfilled:
 - An unused instruction code is detected (see tables with SPI instructions).
 - In case the previous transmission is not completed in terms of internal data processing. (Violation of the minimum Access-Time.)
 - In case of the previous transmission has detected more than 16 SCK pulses
 - Reset has occurred (Undervoltage on DMS)

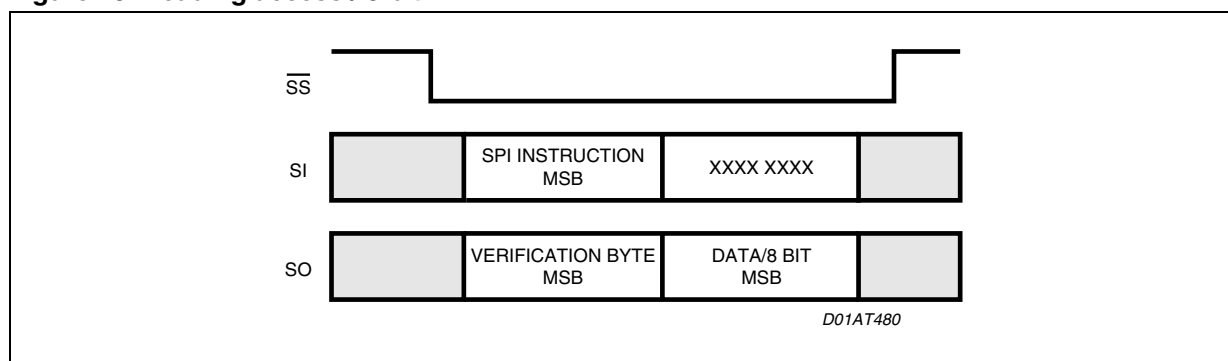
If an invalid instruction is detected, any modifications on registers of L9929 are not allowed.

In case an unused instruction code occurred the databyte "ffh ex" will be transmitted after having sent the check byte.

In addition any access is invalid if the number of SPI clock pulses (falling edge) counted during active SS differs from exactly 16 clock pulses (-> See Note).

5.4 SPI Communication

Figure 13. Reading access / 8 bit



5.5 SPI Instruction

The uppermost 2 bit of the instruction byte contains the chipaddress. The chipaddress of L9929 is 00.

MSB							
7	6	5	4	3	2	1	0
0	0	INSTR5	INSTR4	INSTR3	INSTR2	INSR1	INSR0

SPI Instruction	Encoding		Description
	bit 7,6 CPAD1,0	bit 5,4,3,2,1,0 INSTR(5...0)	
RD_IDENT	00	000 000	Read identifier
RD_VERSION	00	000 011	Read version
RD_DIA	00	001 001	Read DIA_REG
		All others	No function

5.6 Reset of the Diagnostic Register DIA_REG

On the following conditions DIA_REG is reset:

- With the rising edge of the SS-signal after the SPI-Instruction RD_DIA (only if error free while SS, new errors will actualize DIA_REG with the rising edge of SS).
- When the voltage on DMS exceeds the threshold for detecting SPI-Mode. (after undervoltage condition or after power up)
- - If VS rises over about the undervoltage level, the Bits of DIA_REG are restored (when VS internal or DMS > 3,1V)

Verification byte:

MSB							
7	6	5	4	3	2	1	0
Z	Z	1	0	1	0	1	TRANS_F

Bit	Name	Description
0	TRANS_F	Bit = 1: error detected during previous transfer Bit = 0: previous transfer was recognised as valid
1		Fixed to High
2		Fixed to Low
3		Fixed to High
4		Fixed to Low
5		Fixed to High
6		Send as high impedance
7		Send as high impedance

5.7 Diagnostics/Encoding of Failures

Description of the SPI Registers (SPI Instructions: RD_DIA)

Register: DIA_REG							
7	6	5	4	3	2	1	0
Active	OT	CurrRed	CurrLim	DIA21	DIA20	Dia11	DIA10

State of Reset: FFH		
Access by Controller: Read only		
Bit	Name	Description
0	DIA 10	Diagnosis-Bit1 of OUT1
1	DIA 11	Diagnosis-Bit2 of OUT1
2	DIA 20	Diagnosis-Bit1 of OUT2
3	DIA 21	Diagnosis-Bit2 of OUT2
4	CurrLim	Is set to „0“ in case of current limitation
5	CurrRed	Is set to „0“ in case of temperature dependet current limitation
6	OT	Is set to „0“ in case of overtemperature
7	Active	Shows the wired-or state of the Pins EN and DI

Encoding of the Diagnostic Bits of the Output-Stages OUT1 and OUT2				
DIA21	DIA20	DIA11	DIA10	
-	-	0	0	Short circuit over load (SCOL)
-	-	0	1	Short circuit to battery on OUT1 (SCB1)
-	-	1	0	Short circuit to ground on OUT1 (SCG1)
-	-	1	1	No error detected on OUT1
0	0	-	-	Open load
0	1	-	-	Short circuit to battery on OUT2 (SCB2)
1	0	-	-	Short circuit to ground on OUT2 (SCG2)
1	1	-	-	No error detected on OUT2

0	0	0	0	Undervoltage on Pin V _S
---	---	---	---	------------------------------------

Description of DIA_REG Bit7

EN	DI	DIA_REG Bit7
0	0	0
0	1	0
1	0	1
1	1	0

5.8 Device Identifier and Revision Number

The IC's identifier is used for production test purposes and features plug & play functionality depending on the systems software release. It is made up on a device-number and a revision number each one read-only accessible via standardised instructions.

The Device number is defined once to allow indentification of different IC-Types by software.

The Revision number may be utilised to distinguish different states of hardware. The contents is divided into an upper 4 bit field reserved to define revisions correspondending to specific software releases. The lower 4 bit field is utilised to indentify the actual maskset.

Both (SWR and MSR) will start with 0000b and are increased by 1 every time an according modification of the hardware is introduced.

5.9 Reading the IC Identifier (SPI Instruction: RD_IDENT):

IC Identifier1 (Device ID)							
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Bit	Name		Description				
7...0	ID(7...0)		ID-No.: 1010 0001				

5.10 Reading the IC revision number (SPI Instruction: RD_VERSION):

IC's revision number							
7	6	5	4	3	2	1	0
SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0
Bit	Name		Description				
7...4	SWR(3...0)		Revision corresponding to Software release: 0Hex				
3...0	MSR(3...0)		Revision corresponding to Maskset: 8Hex				

Figure 14. Application example with SPI-Interface

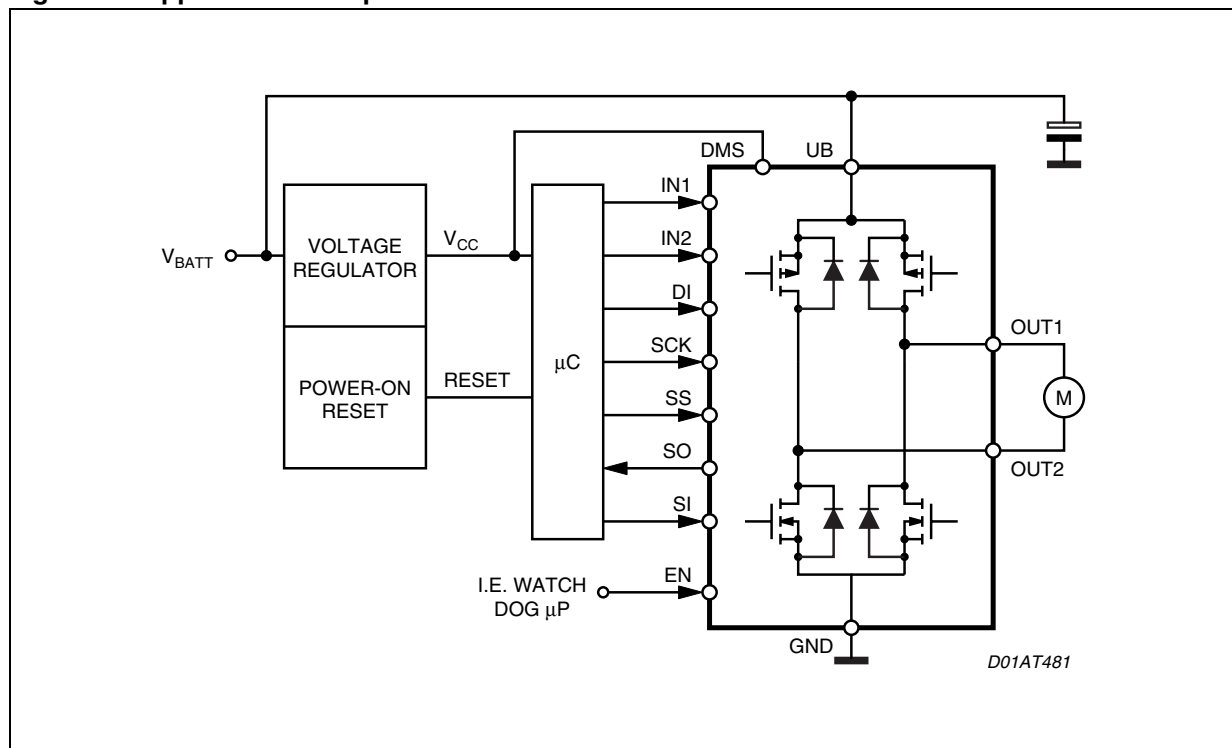


Figure 15. Application example with Status-Flag

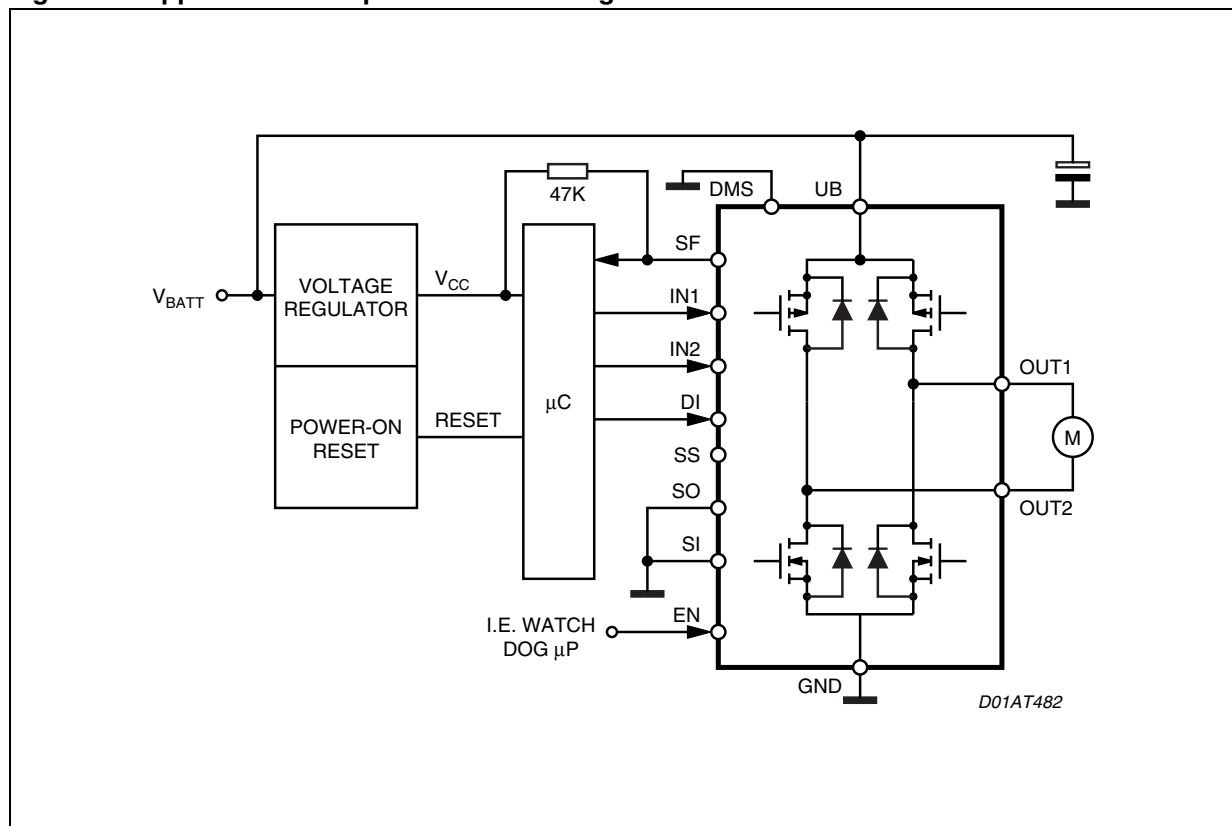
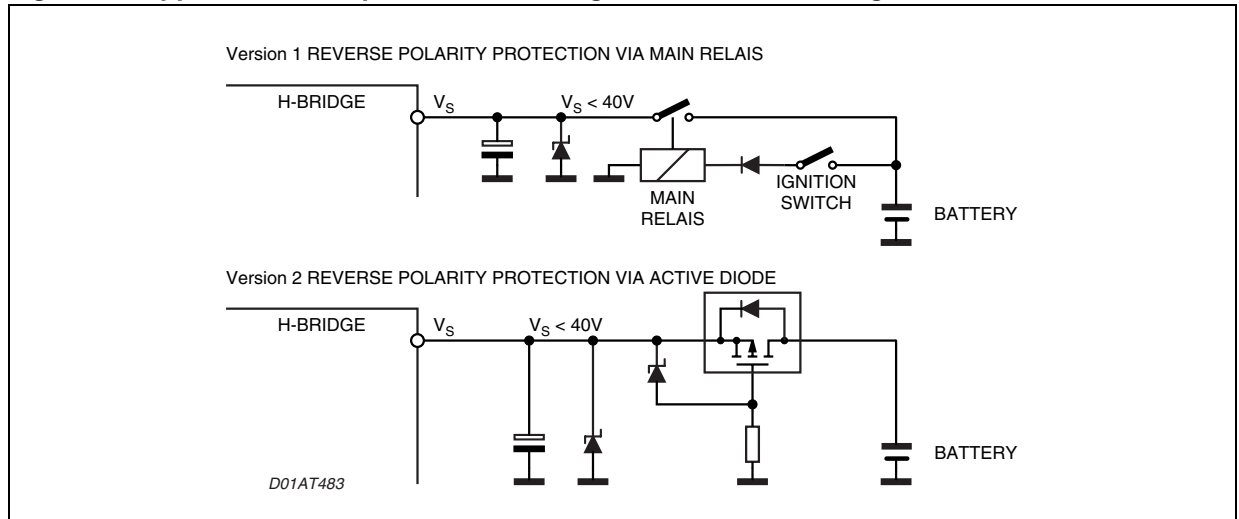


Figure 16. Application examples for Overvoltage- and Reverse-Voltage Protection

6 ESD-SOLIDITY

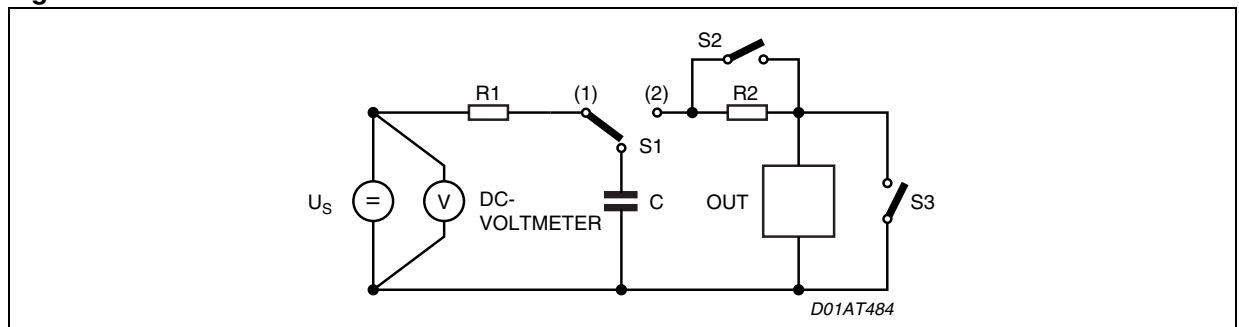
The connection pins of the IC have to be protected against Electrostatic Discharge (ESD) by suitable integrated protection structures.

The integrated circuit has to meet the demand of the „Human-Body-Model“ with $V_C = \pm 4\text{kV}$
 $C = 100\text{pF}$ and $R_2 = 1,5\text{k}\Omega$ (330Ω for OUT1 and OUT2).

Thereby any defect or destruction of the integrated circuit must not occur.

The protection structures realized to reach the ESD-strength have to be coordinated.

The ESD-strength has to be verified by the test circuit given as below.

Figure 17.

For the Pins 4, 5, 6, 7, 14 and 15

$U_C = \pm 4\text{kV}$

$R_1 = 100\text{k}\Omega$

$R_2 = 330\Omega$

$C = 100\text{pF}$

Number of pulses each pin: 18

Frequency: 1Hz

Arrangement and performance:

The requirements of MIL883D Methode 3015 have to be fulfilled.

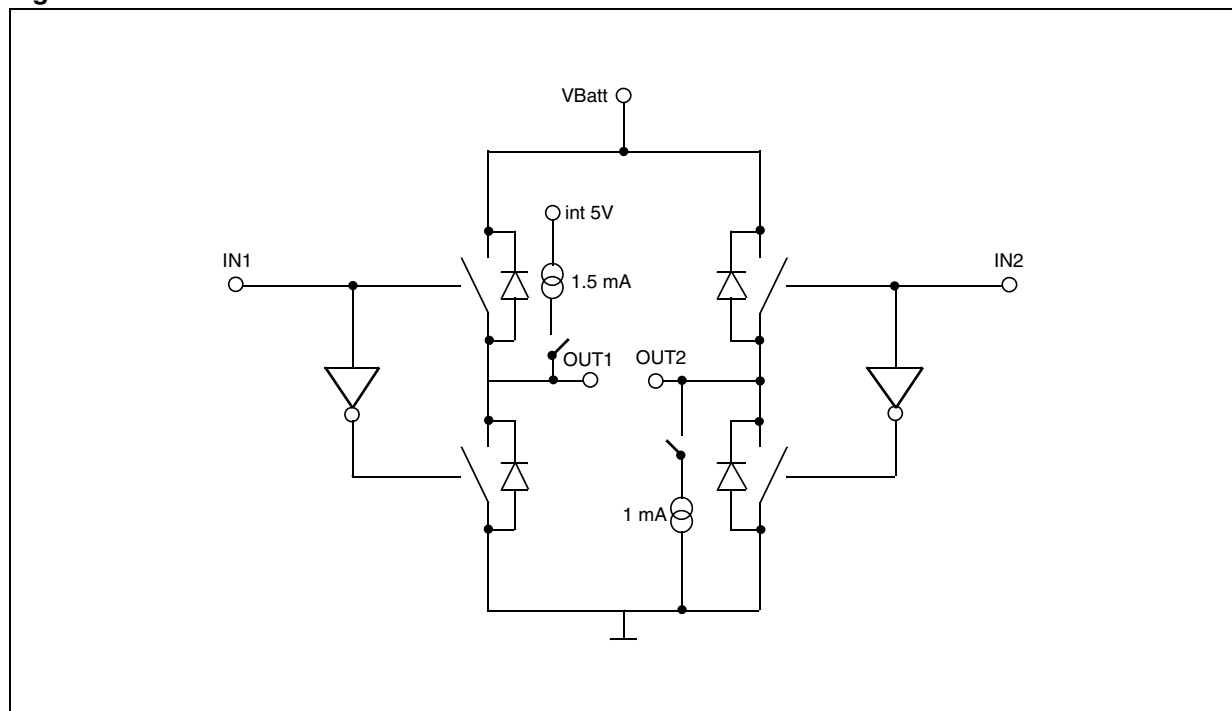
By means of external components (see Fig. 12) the following maximum ratings of the IC will not be exceeded.

dynamical for $t < 500$ ms -2V +40V

APPENDIX A

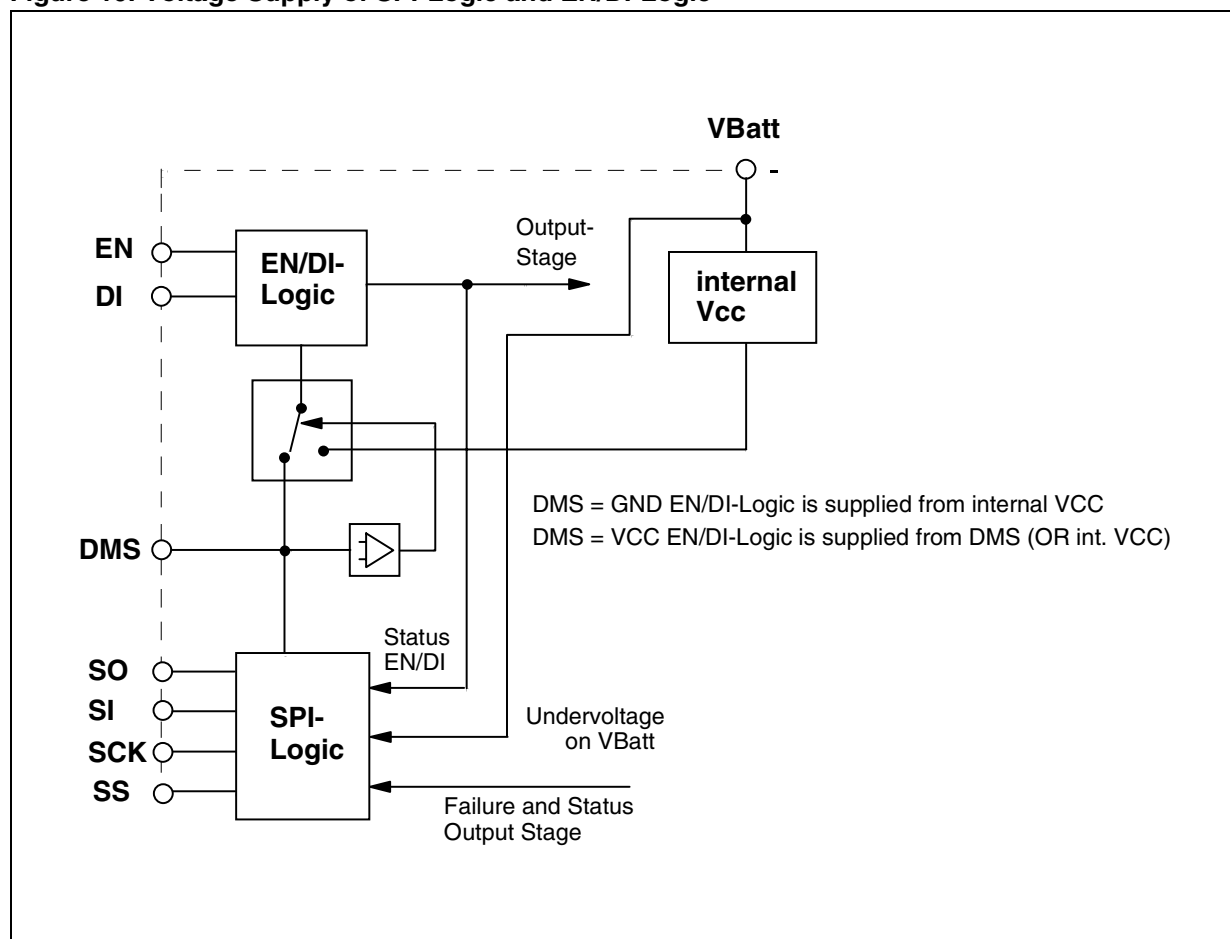
	OUT1	OUT2	
Load available	1	1	
Open Load	1	0	
SC -> GND on OUT1 with Load	0	0	SC detected on normal operation
SC -> GND on OUT2 with Load	0	0	SC detected on normal operation
SC -> UB on OUT1 with Load	1	1	SC detected on normal operation
SC -> UB on OUT2 with Load	1	1	SC detected on normal operation
SC -> GND on OUT1 Open Load	0	0	OL not detected Double Fault
SC -> GND on OUT2 Open Load	1	0	OL detected
SC -> UB on OUT1 Open Load	1	0	OL detected
SC -> UB on OUT2 Open Load	1	1	OL not detected Double Fault

Figure 18.



8 APPENDIX B

Figure 19. Voltage Supply of SPI-Logic and EN/DI-Logic



9 Package Information

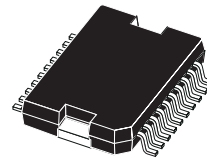
Figure 20. PowerSO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8°(typ.)					
S	8°(max.)					
T		10			0.394	

- (1) "D and E1" do not include mold flash or protrusions.
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")
 - Critical dimensions: "E", "G" and "a3".
 (2) For subcontractors, the limit is the one quoted in jepec MO-166

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO20

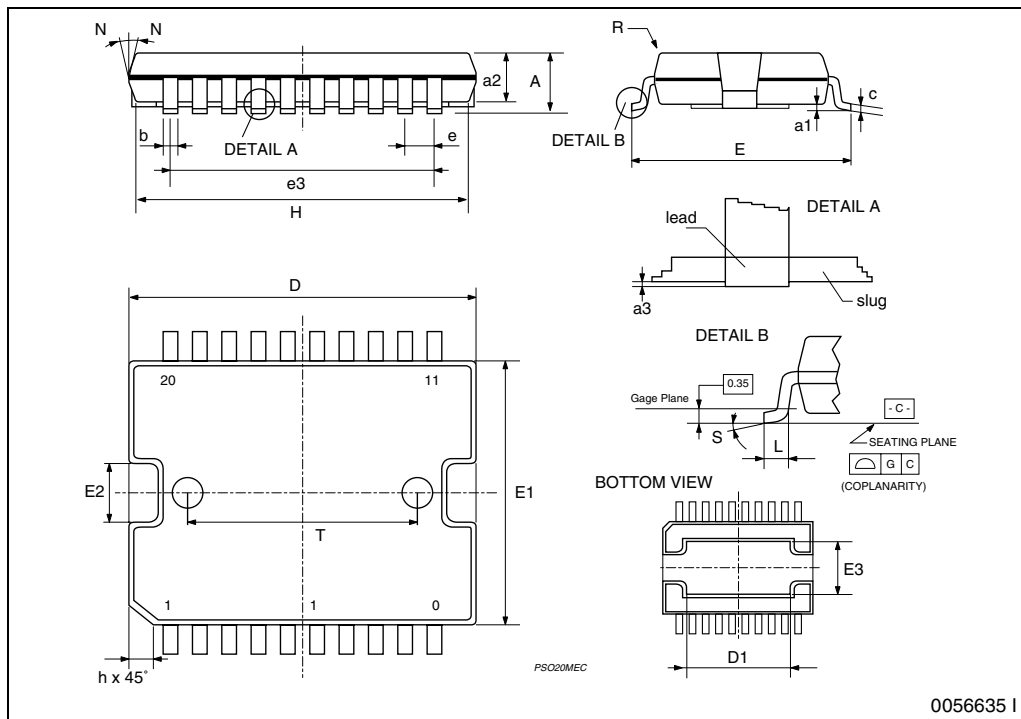


Figure 21. PowerSSO24 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.012
D ⁽¹⁾	10.10		10.50	0.398		0.413
E ⁽¹⁾	7.4		7.6	0.291		0.299
e		0.8			0.031	
e3		8.8			0.346	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
N	10° (max)					
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

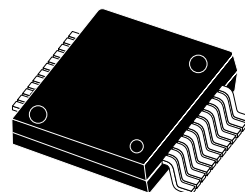
(1) "D and E1" do not include mold flash or protusions.

Mold flash or protusions shall not exceed 0.15mm (0.006")

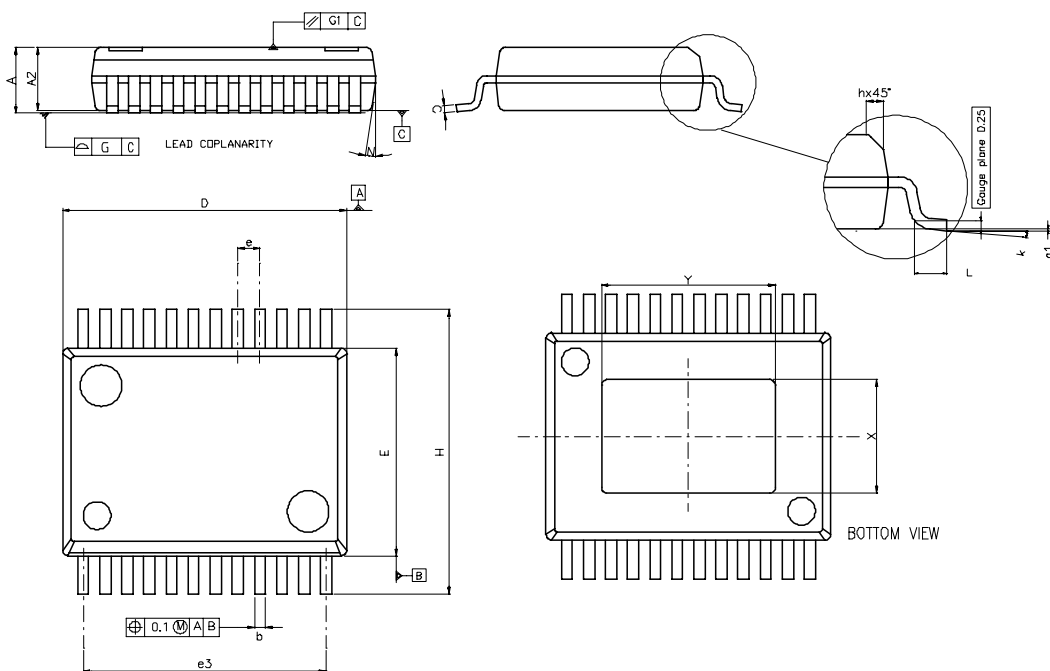
(2) No intrusion allowed inwards the leads.

(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side

OUTLINE AND MECHANICAL DATA



PowerSSO24



7412828 A

10 Revision History

Table 8. Revision History

Date	Revision	Description of Changes
07-Mar-2005	1	First Issue
13-May-2005	2	Add package PowerSSO24

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